

## WHAT IS CLAIMED IS:

1. DC-offset eliminating method for a receiving circuit of a receiver which receives signals comprising a plurality of frames continuously sent to the receiving circuit, each of the frames has a predetermined frame structure and only at the head of each frame a preamble portion is added, comprising the steps of:

calculating a DC-offset component depending upon the received signals;

subtracting said DC-offset component from the received signals; and

performing a DC-offset eliminating operation based on the subtracted result,

wherein in said DC-offset eliminating operation, a DC offset follow-up speed is set for reducing a follow-up speed with respect to the DC offset when said preamble portion is being received, regardless of a time when a continuous reception is performed in which all of said frames are received to recognize the timing of the frame number to be received or a time when an intermittent reception is executed in which only a frame destined for said receiver itself is received.

2. The DC-offset eliminating method according to claim 1, wherein said frames including as said frame structure, an alignment portion, a control portion providing indications of the frame number cyclic at predetermined intervals and of which receiver should receive the frame number, a DATA portion, and a signal-end indication portion showing as to whether other frames continuously follow said frames, and wherein said DC-offset eliminating operation changes over said DC-offset follow-up speed in accordance with a signal obtained by the logical AND operation performed on a frame-continuation detection signal which becomes "1" when said alignment portion is detected from

the received frames and becomes "0" when a signal end contained in said signal-end indication portion is detected, and on a received frame signal which becomes "1" only when the frames destined for said receiver itself.

3. The DC-offset eliminating method according to claim 2, wherein said DC-offset follow-up speed is associated with a predetermined follow-up speed coefficient which takes one of two values, 0 or a positive value.

4. A receiving circuit for eliminating a DC offset comprising:

a detecting circuit for selectively receiving and detecting signals configured by a plurality of frames which are continuously sent to the receiving circuit, each of said frames including an alignment portion, a control portion providing indications of the frame number cyclic at  
predetermined intervals and of which receiver should receive the frame number, a DATA portion, and a signal-end indication portion showing as to whether other frames continuously follow said frames, and at the head of each frame a preamble portion is added;

an analog to digital (A/D) converting circuit for converting said detected signals into digital signals;

a DC-offset eliminating circuit for eliminating a DC-offset component from said converted digital signals;

a demodulating circuit for demodulating said frames from said digital signals from which the DC-offset component has been eliminated;

a control circuit for determining the frame number and which frames should be received, depending upon information input from said control portion so as to turn on the power to said detecting circuit and said A/D converting circuit, thereby outputting a control signal for instructing to receive an appropriate frame, and for outputting to said DC-offset eliminating circuit a received frame signal showing that said

appropriate frame is being received, depending upon information contained in said alignment portion in the received frames; and

an signal-end detecting circuit for outputting a frame-continuation  
 25 detection signal to said DC-offset eliminating circuit by monitoring said information contained in said alignment portion and information contained in said signal-end indication in the received frames,

wherein said DC-offset eliminating circuit includes:

a subtracting circuit for eliminating a DC offset by subtracting a  
 30 calculated DC-offset value from said digital signals, and for outputting the result to said demodulating circuit;

a multiplying circuit for multiplying said output from said subtracting circuit by a coefficient H or L ( $0 \leq L < H$ );

an adding circuit for adding said calculated DC-offset value to an  
 35 output from said multiplying circuit;

a 1-bit delay circuit for delaying an output from said adding circuit by one bit to output said calculated DC-offset value; and

an AND circuit for performing logical AND operation on said received frame signal input from said control circuit and said  
 40 frame-continuation detection signal input from said signal-end detecting circuit,

characterized in that:

said DC-offset eliminating circuit selects any one of said coefficients H and L depending upon an output from said AND circuit.

5. The receiving circuit according to claim 4, wherein said coefficient L takes the value of 0, and said coefficient H takes the value of 1.